Claims

What is claimed is:

1. An integrated circuit, comprising:

a sensor operable to detect performance variations of an individual circuit in said integrated circuit, said performance variation being related to aging of said integrated circuit; and

a compensation circuit operable to change the operating characteristics of said individual circuit to compensate for said performance variation in accordance with an aging-versus time performance curve.

2. The integrated circuit of claim 1, wherein the individual circuit comprises a phase-locked loop.

3. The integrated circuit of claim 2, wherein the compensation circuit comprises a charge pump having multiple legs that can be selectively enabled to change the performance characteristics of said phase-locked loop.

4. The integrated circuit of claim 2, wherein compensation circuit comprises a power supply controlled by digital control words to selectively change the operating characteristics of said phase-locked loop.

5. The integrated circuit of claim 2, comprising a ring oscillator operable to approximate the effects of NBTI and to generate a compensation signal corresponding thereto.

6. The integrated circuit of claim 5, wherein said compensation signal is used to generate digital control words to control operation of a power supply.

7. The integrated circuit of claim 6, wherein said power supply is operable to control operation of a voltage controlled oscillator in said phase-locked loop.

8. The integrated circuit of claim 1, wherein said individual circuit is a delay-locked loop.

9. The integrated circuit of claim 8, wherein the compensation circuit comprises:

a dummy delay line operable to generate a dummy delay line clock signal;

a reference source operable to generate a reference clock signal; and

a comparator operable to compare the dummy delay line clock signal and the reference clock signal and to generate a control signal therefrom.

10. The integrated circuit of claim 9, further comprising a power supply controller operable to control operation of the delay line of said delay-locked loop in response to said control signal.

11. The integrated circuit of claim 10, wherein said power supply controller controls operation of said delay line by generating a digital power supply control word (VDD_DLL).

12. A method for controlling operation of an integrated circuit, comprising:

detecting performance variations of an individual circuit in said integrated circuit, said performance variation being related to aging of said integrated circuit; and

generating a compensation signal to change the operating characteristics of said individual circuit to compensate for said performance variation in accordance with an aging-versus time performance curve.

13. The method of claim 12, wherein the individual circuit comprises a phase-locked loop.

14. The method of claim 13, wherein said compensation signal is generated by a charge pump having multiple legs that can be selectively enabled to change the performance characteristics of said phase-locked loop.

15. The method of claim 13, wherein compensation signal is generated by a power supply controlled by digital control words to selectively change the operating characteristics of said phase-locked loop.

16. The method of claim 13, wherein said compensation signal is generated by a ring oscillator operable to approximate the effects of NBTI and to generate a compensation signal corresponding thereto.

17. The method of claim 16, wherein said compensation signal is used to generate digital control words to control operation of a power supply.

18. The method of claim 17, wherein said power supply is operable to control operation of a voltage controlled oscillator in said phase-locked loop.

19. The method of claim 12, wherein said individual circuit is a delay-locked loop.

20. The method of claim 19, wherein the compensation circuit comprises:
a dummy delay line operable to generate a dummy delay line clock signal;
a reference source operable to generate a reference clock signal; and
a comparator operable to compare the dummy delay line clock signal and the reference clock signal and to generate a control signal therefrom.